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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,293	CHAPEK, DAVID L.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art with Henley et al. (U.S. Patent No. 6083324).

With regard to claim 9, Burns et al. teach in figure 9.8 on page 381 a semiconductor substrate, a silicon dioxide layer formed on the substrate, and a layer of polycrystalline silicon formed on the layer of silicon dioxide. Burns et al. do not teach the surface of the layer of silicon dioxide having hydrogen ions implanted therein and being free of sputtered metal contaminants or the layer of polycrystalline silicon having a smooth morphology.

Applicant's admitted prior art teaches on page 1 lines 5-22 a layer of silicon dioxide wherein the surface of the layer of silicon dioxide has been doped with hydrogen ions so that a layer of polycrystalline silicon formed thereon will have a smooth morphology. The admitted prior art does not teach the layer of silicon dioxide being free of sputtered metal contaminants as the Kaufman ion source causes metal contaminants in the layer. The admitted prior art teaches the metal contaminants being produced

from metal sputtering off a metal grid in the Kaufman ion source apparatus and that as device sizes decrease the effect of the damage from the metal contaminants increases.

Henley et al. teach a plasma immersion ion implantation apparatus that can be used for implanting hydrogen ions into semiconductors. It is noted that plasma source ion implantation (PSII or PSI) and plasma immersion ion implantation (PIII) are interchangeable terms for the same plasma treatment. Henley et al. teach that their implantation method can be used on SOI (silicon-on-insulator) substrates in column 2 lines 30-40 and teach implanting hydrogen ions in line 38, for example.

Applicants admitted prior art and Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant the hydrogen using the PSII technique of Henley et al. The motivation for doing so is to that PIII is cost effective, easy to use, and produces less impurity metal contamination (Henley et al. column 3 lines 12-17). Therefore, it would have been obvious to combine Applicant's admitted prior art with Henley et al. to alleviate the metal contamination.

Burns et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the surface of the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art and Henley et

al. to obtain the invention of claim 9. In the combination of the references, the layer of polycrystalline silicon formed on the layer of silicon dioxide would have a smooth morphology.

With regard to claim 10, Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, a silicon dioxide layer formed on at least a portion of the substrate, a layer of polycrystalline silicon formed on at least a portion of the silicon dioxide layer, and a gate oxide formed on the substrate from the layer of silicon dioxide, and a source and a drain in the substrate where a gate electrode is formed on the substrate from the layer of polycrystalline silicon. Burns et al. do not teach the surface of the layer of silicon dioxide having hydrogen ions implanted therein or being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into the surface of a layer of silicon dioxide on page 1 lines 12-16 and Henley et al. teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the gate oxide would be formed from the layer of silicon dioxide having hydrogen ions implanted therein and the layer of polycrystalline silicon formed on the layer of silicon dioxide would have a smooth morphology.

Burns et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into

the surface of the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon. The gate oxide for each transistor of the combination of references would be formed of the silicon dioxide having hydrogen atoms implanted the surface therein as taught above with regard to claim 10.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon. As evidence that is it well known in the art at the time of the invention that a wafer is divided into a

plurality of die see Wolf et al. In figure 3, Wolf et al. shows an entire wafer processed (in the wafer processing steps), probed, and then diced into ~50 to 1000 chips. Thus, Wolf et al. is direct evidence that it is obvious to split a wafer into a plurality of chips.

3. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art with Henley et al. as applied to claims 9-12 above.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate 501 of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a gate oxide formed from the insulating layer, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the surface of the substrate having hydrogen ions implanted therein or the substrate being free of sputtered metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into the surface of a layer of silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Henley et al. as discussed above teach using a PSII method to implant the hydrogen. Applicant's admitted prior art with Henley et al. as discussed above also teach the silicon dioxide as being free of sputtered metal contaminants. In the combination of the references, the layer of polycrystalline silicon formed on the layer of substrate would have a smooth morphology.

Murata et al. and Applicant's admitted prior art with Henley et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the surface of the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art and Henley et al. to obtain the invention of claim 14.

Response to Arguments

4. Applicant's arguments filed 11/15/04 have been fully considered but they are not persuasive.

Applicant has first argued that Henley et al. provide no motivation for implanting hydrogen ions on the surface of a silicon dioxide layer for the purpose of providing a smooth morphology for a layer of polycrystalline silicon formed on the silicon dioxide layer. Henley et al. was not relied upon to teach this combination of limitations, but merely to teach an alternate ion implantation method than that of the admitted prior art to specifically overcome the metal contamination of the prior art. Arguing that Henley et al. alone does not teach a combination of limitations that Henley et al. was not relied upon to show is irrelevant to the rejection based upon the combination of references above.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant further argues that Henley et al. teach implanting ions beneath the surface and not into the surface of a silicon dioxide layer. This is not persuasive as Henley et al. was not specifically relied upon to teach implanting ions into the surface of a silicon dioxide layer. Rather, the admitted prior art teaches implanting hydrogen ions into the surface of a silicon dioxide layer. The admitted prior art teaches a specific method for performing the ion implantation, specifically using a Kaufman ion source. However, the admitted prior art also teaches that the Kaufman source causes undesirable metal contamination. Henley et al. is relied upon to teach an alternate method for ion implantation, specifically PIII. Henley et al. not only address and solve applicants recognized contamination problem but also provide motivation as to why one of ordinary skill in the art would use PIII to implant ions apart from solving the contamination problem. Henley et al. teach on column 3 lines 13-17 that PIII is an improved processing technique that is cost effective, easy to use and produces less metal impurity contamination than other ion implantation techniques. Thus, Henley et al. has solved applicant's recognized problem and provided specific motivation to use the PIII technique instead of the Kaufman source implantation of the admitted prior art.

The combination of applicants admitted prior art with Henley et al. teaches implanting hydrogen ions into the surface of a layer of silicon dioxide as claimed. In the combination, using PIII to implant the hydrogen ions, the layer would be free of metal contaminants. In all, the arguments are not persuasive.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited as they teach that PSII and PIII are known in the art to be refer to the same implantation technique. The references are provided in case evidence is later needed as a factual showing that PSII and PIII are the same. Goechner et al. (U.S. Patent No. 6,335,536 B1), Gaudreau et al. (U.S. Patent No. 6,368,676 B1), Todd (U.S. Publication No. 2002/0173113 A1).

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

GEORGE ECKERT
PRIMARY EXAMINER